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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,621	03/18/2004	Michael Page	282569US8X	5821

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OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
05/16/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/803,621	PAGE, MICHAEL	
	Examiner	Art Unit	
	JASON M. PERILLA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,9 and 13-24* is/are rejected.

7)☒ Claim(s) *7,8 and 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 and 3-24 are pending in the instant application.

Response to Amendment/Argument

2. The Applicant's remarks filed April 14, 2008, have been fully considered.

Upon further search and consideration, new prior art rejections are set forth below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-6, 9, and 13-24 are rejected under 35 U.S.C. § 102(b) as being anticipated by Page ("MAC-DSD Multi-channel Audio Connection for DSD", version 1.1, November 1, 2002 – 2004 IDS Paper Ref. "AR").

Regarding claim 1, Page discloses, according to figures 2, 3, and 5, a data communications system for communicating a data signal ("DSD") formed of successive data elements, said system comprising a transmission node (fig. 2), a reception node (fig. 3), and a link ("Category 5 cable") providing a data connection from said transmission node to said reception node; said transmission node comprising: a clocking-signal transmitter (fig. 2, "Low-pass filter", "Differential line driver", and "Clock") configured to transmit a synchronization clocking signal to said reception node via said link, said synchronization clocking signal having synchronizing features occurring at a

frequency lower (i.e. 64fs) than a data element rate (i.e. fig. 5; 24DSD channels x 64fs = payload of 67.7Mbit/s); and an assembler (figs. 2 or 5, "PHY") configured to assemble elements of said data signal into data frames, each data frame having a plurality of successive data elements of said data signal, for transmission to said reception node via said link, said assembler being responsive to said synchronization clocking signal (fig. 5, ref. "PLL") so as to set a synchronization or "frame" flag associated with a data frame containing a data element (i.e. "associated with "First DSD sample"; pg. 14, see description of "Frame Flag") having a first predetermined temporal relationship with a synchronizing feature of said synchronization clocking signal (pg. 14, "Frame Types" and "Frame Flags"; pg. 18) and to position such a data element at a predetermined position within the data frame (pgs. 12-13; Bits 15:12); and said reception node (fig. 3,) comprising: a detector (fig. 3, "Comparator") for configured to detect a synchronizing feature of said synchronization clocking signal received from said transmission node; a disassembler (fig. 3, "PHY") configured to disassemble received data frames to regenerate said data signal, said disassembler being operable to detect a data element associated with a set synchronization flag (pg. 18); an output unit (fig. 3, "MAC-DSD") configured to output a data element associated with a set synchronization flag at a second predetermined temporal relationship with respect to said synchronizing feature of said received synchronization clocking signal (pg. 12); wherein said first and second predetermined temporal relationships are arranged so that a predetermined system latency exists between input of a data element to said transmission node and subsequent output of that data element by said reception node (pg. 13). .

Regarding claim 3, Page discloses the limitations of claim 1 as applied above. Further, Page discloses that the predetermined position is a first transmitted data element within the data frame. On pages 12-13, Page discloses that bits 15:12 are "frame flags". Page discloses that they are "first" in a transmitted data frame because, on page 12, they occur first (i.e., from right to left, "Flags, Frame Type, Protocol Major Ver., Protocol Minor Ver.").

Regarding claim 4, Page discloses the limitations of claim 1 as applied above. Further, Page discloses that said transmission node (fig. 2) comprises a data clock transmitter (fig. 2, "Clock") for transmitting a data clock to said receiving node via said link (fig. 2, "Category 5 cable"), said data clock defining said timing of said data elements or components of said data elements (as applied above); and said reception node (fig. 3) comprises a data clock receiver (fig. 3, "Clock") for receiving said data clock from said transmitting node and for outputting said data elements in accordance with said received data clock.

Regarding claim 5, Page discloses the limitations of claim 4 as applied above. Further, official notice is taken that said data clock transmitter is configured to transmit a Multipoint Low-Voltage Differential Signaling signal to said receiving node. Specifically, Page discloses use of the "100Base-TX physical layer of Fast Ethernet IEEE802.3" standard (pg. 3) which utilizes low voltage differential signaling.

Regarding claim 6, Page discloses the limitations of claim 4 as applied above. Further, Page discloses that said transmission node (fig. 2) comprises a combiner (fig. 2, "RJ45") configured to combine said synchronization clocking signal (fig. 2, "Clock")

and said data clock (fig. 2, "Data") to form a multiplexed clock signal for transmission to said reception node via said link (fig. 2, "Category 5 cable"); and said reception node (fig. 3) comprises a demultiplexer (fig. 3, "RJ45") configured to demultiplex said synchronization clocking signal (fig. 3, "Clock") and said data clock (fig. 3, "Data") from said multiplexed clock signal.

Regarding claim 9, Page discloses the limitations of claim 1 as applied above. Further, Page discloses that the transmission note is responsive to an externally supplied synchronization clocking signal (fig. 4, "Clock source/PLL").

Regarding claims 13-17, Page discloses the limitations of claim 1 as applied above. Further Page discloses the remaining limitations of the claims as provided in the "Clock Transfer Specifications" section (pgs. 20-23).

Regarding claim 18, Page discloses the limitations of claim 4 as applied above. Further, Page discloses that said data clock (fig. 2, "Clock") defines the timing of individual data bits of each word; said transmission node (fig. 2) and reception node (fig. 3) operate in accordance with a word clock (fig. 5, "64Fs clock"), being a sub-multiple of said data clock (fig. 5, "576fs clock"), to define the timing of individual data words.

Regarding claim 19, Page discloses the limitations of claim 18 as applied above. Further, Page discloses that said synchronizing feature of said synchronization clocking signal has a constant temporal relationship (via the PLL; fig. 5, "PLL") to said word clock.

Regarding claim 20, Page discloses the limitations of claim 19 as applied above. Further, Page discloses that said reception node comprises a word clock extractor (fig.

4, "Lock detect") configured to derive said word clock from said synchronizing features of said synchronization clocking signal.

Regarding claim 21, Page discloses the limitations of claim 1 as applied above. Further, Page discloses that said link is a wired link (fig. 2, "Category 5 cable").

Regarding claim 22, Page discloses the limitations of claim 1 as applied above. Further, Page discloses that said link comprises the physical layer of an Ethernet link (pg. 3, "Introduction").

Regarding claim 23, Page discloses a transmission node (fig. 8, "Transmitter") for use in a data communications system for communicating a data signal formed of successive data elements having a reception node (fig. 8, "Receiver") and a link (fig. 8, "twisted pair cable") providing a data connection from said transmission node to said reception node, said transmission node comprising: a clocking signal transmitter (fig. 2, "Clock") configured to transmit synchronization clocking signal to said reception node via said link, said synchronization clocking signal having synchronizing features occurring at a frequency lower than a data element rate (see application in claim 1 above); and an assembler (fig. 8, "Assemble Frame") configured to assemble elements of said data signal into data frames, each data frame having a plurality of successive data elements of said data signal, for transmission to said reception node via said link, said assembler being responsive to said synchronization clocking signal so as to set a synchronization flag or "frame flag" (see application in claim 1 above) associated with a data frame containing a data element having a first predetermined temporal relationship with a synchronizing feature of said synchronization clocking signal and to position such

a data element at a predetermined position within the data frame (see application in claim 1 above).

Regarding claim 24, Page discloses a reception node (fig. 8, "Receiver") for use in a data communications system for communicating a data signal formed of successive data elements having a transmission node (fig. 8, "Transmitter") and a link (fig. 8, "twisted pair cable") providing a data connection from said transmission node to said reception node, said reception node comprising: a synchronization detector (fig. 3, "Comparator") configured to detect a synchronizing feature of said synchronization clocking signal (fig. 3, "Clock") received from said transmission node, said synchronization clocking signal having synchronizing features occurring at a frequency lower than a data element rate (see application in claim 1 above); a disassembler (fig. 8, "Disassemble frame") configured to disassemble received data frames to regenerate said data signal, said disassembler configured to detect a data element associated with a set synchronization flag (pg. 18, "Frame Synchronization across multiple links"); and an output unit (fig. 8, "Decode parity and extract data from block") configured to output a data element associated with a set synchronization flag at a second predetermined temporal relationship with respect to said synchronizing feature of said received synchronization clocking signal (pg. 18-19), said output unit comprising a time delay arrangement so that data elements from a data frame associated with a set synchronization flag are output at a predetermined delay time after said reception node receives said synchronizing feature of said synchronization clocking signal.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Page.

Regarding claim 3, Page discloses the limitations of claim 1 as applied above. Page discloses that the synchronization or "frame flag" is positioned at a predetermined position within the data frame as applied to claim 1 above (see also rejection of claim 3 above). Moreover, even if Page's disclosure with respect to the position of the frame flags within the data frame is not deemed a sufficient disclosure of the claimed limitation that the predetermined position is a first-transmitted data element position within the data frame, the limitation is still considered obvious. The placement of the frame flag at any appropriate position within the data frame would have been an obvious matter of design choice to one having ordinary skill in the art. The specification of the instant application does not disclose that any particular advantage (i.e. synergy) is accomplished by placing the frame flag at a first-transmitted data element position, and one skilled in the art would have found it obvious to choose any appropriate position because the positioning of the frame flag at any position in the data frame would have led to predictable and expected results.

Allowable Subject Matter

7. Claims 7, 8, and 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M Perilla/
Primary Examiner, Art Unit 2611
May 10, 2008

/jmp/